

SEMICONDUCTOR DEVICES AND MANUFACTURING METHODS

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5 This application is a Divisional of U.S. Application Serial No. 09/178,875, filed Oct.
26, 1998, ^{PAT 6,696,733} which is hereby incorporated by reference in its entirety.

Technical Field

Embodiments of the present invention relate to semiconductor devices such as an
10 integrated circuit having active and passive elements.

Related Art

In a conventional semiconductor device such as an integrated circuit, a diffusion
layer or a polysilicon layer formed on a semiconductor substrate has been commonly used as
15 an electrode for forming a capacitive element.

However, the aforementioned electrode comprising a diffusion layer or polysilicon
layer forms an obstacle for high-speed operation of an integrated circuit because of a large
resistance and a large parasitic capacity. The conventional electrode of a capacitive element
is formed from a different material than that used for a resistance element or a fuse element,
20 and is formed using a process different than that used for forming the resistance element or
the fuse element. This results in complicated manufacturing steps for fabricating the
semiconductor device and increased cost.

Summary

25 It is an object of embodiments of the present invention to solve the aforementioned
problems in the conventional art and to reduce the parasitic capacity of an electrode for a
capacitive element.

Another object of the invention is to simplify the manufacturing process and reduce
manufacturing costs.